IN THE CLAIMS

1 (Original) A power semiconductor device comprising a two-dimensional array of individual cells formed on a semiconductor substrate, each individual cell having source regions within base regions in the semiconductor substrate,
characterised in that the source regions of the individual cells of the array comprise a plurality of source region branches each extending radially towards at least one source region branch of an adjacent cell, the source region branches of adjacent cells presenting juxtaposed ends, the base regions of the individual cells of the array comprising a corresponding plurality of base region branches extending radially towards at least one base region branch of an adjacent cell, and the base region branches of adjacent cells merging together adjacent and between said juxtaposed ends to form a single and substantially uniformly doped base region surrounding said source regions of the individual cells of said array.

2 (Original) The power semiconductor device according to claim 1 wherein said plurality of radially extending branches of an individual cell intersect at a central enlarged area having contact cut-out portions whose width is larger than the width of said radially extending branches.

3 (Original) The power semiconductor device according to claim 2 wherein the cut-out portions of said enlarged area are straight segments or concave curves with an inverse curvature radius.

4 (Currently amended) The power semiconductor device according to ~~any one of the previous claims~~ claim 1 wherein said radially extending branches of each individual cell are linear or non-linear, with constant width or variable width.

5 (Currently amended) The power semiconductor device according to ~~any one of the previous claims~~ claim 1 wherein each individual cell has at least three radially extending branches arranged in such a way that the area defined by the merging adjacent branches is a polygon.

6 (Currently amended) The power semiconductor device according to ~~any preceding~~ claim 1 and comprising at least one drain electrode contacting a face of said semiconductor substrate opposite said source regions.

7 (Currently amended) The power semiconductor device according to ~~any of claims 1 to 5~~ claim 1 further comprising physically isolated drain regions in the substrate and wherein said physically isolated drain regions have a depth equivalent to the depth of said base regions.

8 (Original) The power semiconductor device according to claim 7 wherein said individual cells forming a plurality of source regions and separating said physically isolated drain regions are packed into a relatively small area to contain at least 10 physically isolated drain regions.

9 (Currently amended) The power semiconductor device according to ~~any preceding~~ claim 1 wherein said cells of said array form field effect transistors.

10 (Original) A method for manufacturing a power semiconductor device comprising the steps of:

forming a two-dimensional array of individual cells on a semiconductor substrate, each individual cell having source regions within base regions in the semiconductor substrate, characterised in that the source regions of the individual cells of the array comprise a plurality of source region branches each extending towards at least one source region branch of an adjacent cell, the source region branches of adjacent cells presenting juxtaposed ends,

the base regions of the individual cells of the array comprising a corresponding plurality of base region branches extending radially towards at least one base region branch of an adjacent cell, and the base region branches of adjacent cells merging together adjacent and between juxtaposed ends to form a single and substantially uniformly doped base region surrounding said source regions of the individual cells of said array.

11 (Original) A method for manufacturing a power semiconductor device as claimed in claim 10 comprising the steps of:

forming said base regions extending from a first surface of said semiconductor substrate with radially extending base region branches;

forming said source region within each base region of each individual cell with said radially extending source region branches;

forming a gate oxide region over said first surface;

forming a source electrode in contact with said source regions of each individual cell within each of the plurality of the base regions; and

forming a drain electrode in contact with a second surface of said semiconductor substrate opposite to said first surface.

12 (Original) A method for manufacturing a power semiconductor device as claimed in claim 10 comprising the step of forming in said first surface physically isolated drain surface regions surrounded by said plurality of base regions.

13 (Currently amended) The method of manufacturing a power semiconductor device according to ~~any of claims 10 to 12~~ claim 10 wherein forming said base regions comprises the step of merging said base regions of each individual cell so as to form a single base region.

14 (Currently amended) The method of manufacturing a power semiconductor device according to ~~any of claims 10 to 13~~ claim 10 wherein forming said base regions comprises the step of making ion implant of high voltage breakdown resistance for the base regions before forming a source electrode over said first surface.